MULTIPLE PASS OPTIMIZATION FOR AUTOMATIC ELECTRONIC CIRCUIT PLACEMENT

ABSTRACT

A computer implemented process for the automatic creation of integrated circuit (IC) geometry including a multiple pass process flow using multiple passes of direct timing driven placement after a first pass of non-direct timing driven placement. First, a high level description of the circuit design may be synthesized. Next, a non-direct timing driven placement process may place the design. Then the placed design may be routed. Alternatively, routability may be estimated. After routing, a modified design may be resynthesized. The resynthesized design may then be placed according to a direct timing driven placement process. This sequence may be repeated several times.